CSc 33200-0460: Operating System - Fall 2003

Assignment I

September 03, 2003

Name:_____

ID:_____

- Try to answer all the questions.
- Every question is worth 20 points. For multi-part questions, the 20 points are divided evenly among the parts.
- Write your answer only within the given space using a readable text with normal size font.
- Don't guess! You get 20% of the value of you leave the answer blank. You get no points for a wrong answer.
- You have about one hour.

Good luck!

1. The following recursive function $f(x, y)$ gets as an input two integers $x>0$ and $y>0$:

   $f(x, y)$
   (1) if $x = y$ then return x
   (2) if $x < y$ then $x \leftrightarrow y$
   (3) return $f(x-y, y)$

   a) What is the output for

   $f(27, 15)$ _____ $f(15, 27)$ _____ $f(24, 90)$ _____ $f(21, 13)$ _____

   b) What is $f(x, y)$ computing?

   c) What happens if line (3) becomes: (3) return $f(y, x-y)$

   d) What is the worst case value of y for a given x?

2. Please name at least 3 sorting methods, describe briefly how they work, and give the detailed process of one of them in any programming language you prefer (don't worry about the 100% accuracy of the grammar). Suppose the input is an array of integer, A[1..n], and after the process, it is guaranteed that $A[1] \leq A[2] \leq ... \leq A[n]$.

3. Please explain the function of the following set of micro-operations:

t0: MAR ← (PC)
t1: IR ← (MDR), PC ← (PC+1)
t2: Decoder ← (IR)
t3: ABUS ← (R1), BBUS ← (R2)
t4: ALU ← (R1+R2)
t5: CBUS ← (ALU)
t6: R1 ← CBUS

4.

a) Four 256×8 PROM chips are used to produce a total capacity of 1024×8. How many address bus lines are required?

b) A computer with a 32-bit word size uses 2's complement to represent numbers. What is the range of integers that can be represented by this computer?

5.

a) The Pumpkin Computer uses a segmented addressing scheme in which individual bytes are accessed by combining a 16-bit segment paragraph and a 16-bit relative offset. SR is 16-bit register that points to the beginning of a 16-byte paragraph that is evenly divisible by 16. The segment paragraph is treated as if it were shifted left by four bits. SI is a 16-bit segment index register that contains a relative offset from the segment paragraph specified in SR. What will be the actual memory address accessed if the contents of SR are 1234H and the contents of SI are 4392H?

b) The Mellon Computer can execute 1,000,000 instructions per second. A program running on this computer performs on average a one sector read and a one sector write for every 200 instructions that it executes. The disk drive handling the I/O transfers requires 0.00010 seconds each to perform the read and write operations. Assuming no overlap of these operations, what is the percent of CPU time spent in the wait state?