Assignment 02

Due on 09/22/2003

NOTE: 1. You may find the list of reading materials numbered in order at the course web page. 2. A number in x.x format preceding a problem, like 1.3, indicates the problem is from our textbook.

1. (**1.3**) Consider a hypothetical 32-bit microprocesser having 32-bit instructions composed of two fields: The first byte contains the opcode and the remainder an immediate operand or an operand address.

   a. What is the maximum directly addressable memory capacity (in bytes)?

   b. Discuss the impact on the system speed if the microprocesser bus has

      (a) a 32-bit local address bus and a 16-bit local data bus, or

      (b) a 16-bit local address bus and a 16-bit local data bus.

   c. How many bits are needed for the program counter and the instruction register?

2. (**1.9**) A computer consists of a CPU and an I/O device D connected to main memory M via a shared bus with a data bus width of one word. The CPU can execute a maximum of 106 instructions per second. An average instruction requires five processer cycles, three of which use the memory bus. A memory read or write operation uses one processer cycle. Suppose that the CPU is continuously executing "background" programs that require 95% of its instruction execution rate but not any I/O instructions. Assume that one processer cycle equals one bus cycle. Now suppose that very large blocks of data are to be transferred between M and D.

   a. If programmed I/O is used and each one-word I/O transfer requires the CPU to execute two instructions, estimate the maximum I/O data transfer rate, in words per second, possible through D.

   b. Estimate the same rate if DMA transfer is used.

3. Read **Readings 01**, an article titled *Faster Computing through Software-Controlled Cache Replacement*, and summarize its main idea in your own words.